What is claimed is:

1. A network switch comprising:

at least one port data port interface;

a first memory;

a second memory; and

a memory management unit in connection with said at least one data port interface, said first memory, and said second memory,

wherein the memory management unit receives data from the at least one data port interface, determines if the data is to be stored in one of the first memory or the second memory, stores the data in one of the first memory or the second memory as a linked list, retrieves the data from one of the first memory or the second memory, and forwards the data for egress.

2. A network switch as recited in claim 1, said network switch further comprising

a status location budget manager in connection with the at least one data port interface, the first memory, and the second memory, for determining if the data is to be stored in the first memory or the second memory.

3. A network switch as recited in claim 1, said network switch further comprising

a first memory controller for storing data within said first memory and a second memory controller for storing data within said second memory.

4. A network switch as recited in claim 1, wherein said first memory further comprises on-chip memory.

5. A network switch as recited in claim 1, wherein said second memory further comprises off-chip memory.

6. A network switch as recited in claim 1, wherein the memory management unit further comprises:

a communication channel;

a data input section in connection with the communication channel;

a data output section in connection with the communication channel;

a first memory controller in connection with the first memory, the data input

section, and the data output section;

a second memory controller in connection with the second memory, the data input section, and the data output section;

at least one address pool in connection with the first memory controller and the second memory controller; and

a scheduler in connection with the data input section and the data output section.

7. A network switch as recited in claim 6, wherein the data input section further comprises:

a cell assembly unit in connection with the communication channel;

a status location budget manager in connection with the cell assembly unit;

at least one cell accumulation buffer in connection with the status location budget manager;

a slot assembly unit in connection with the at least one cell accumulation buffer and said second memory controller; and

at least one address pool in connection with the status location budget manager, the slot assembly unit, and the data output section.

8. A network switch as recited in claim 7, wherein the cell assembly unit converts data received from the communication channel into a cell header format, a cell data format, and a sideband information format.

9. A network switch as recited in claim 7, wherein the status location budget manager determines whether data received by the cell accumulation buffer is to be stored in the first memory or the second memory.

10. A network switch as recited in claim 7, wherein the at least one cell accumulation buffer collects data to be stored in the second memory prior to sending the data to be stored in the second memory to the slot assembly unit.

11. A network switch as recited in claim 7, wherein the slot assembly unit receives cells from the cell accumulation buffer and packages the received cells into cell slots to be stored in the second memory.

12. A network switch as recited in claim 6, wherein the data output section further comprises:

a cell disassembly unit in communication with the communication channel;

a cell retrieval and reclaim unit in communication with the cell disassembly unit; and

a read buffer and slot disassembly unit in communication with the cell retrieval and reclaim unit and the second memory controller.

13. A network switch as recited in claim 12, wherein the cell disassembly unit converts a cell format from a CBP format to a CP bus format and transmits a cell to the communication channel when enabled to do so.

14. A network switch as recited in claim 12, wherein the cell retrieval and reclaim unit receives egress for cells and schedules cell egresses through the cell disassembly unit in accordance with a predetermined algorithm.

15. A network switch as recited in claim 14, wherein the predetermined algorithm

further comprises a token order.

16. A network switch as recited in claim 12, wherein the read buffer and slot disassembly unit reads slots from the second memory and sends the slots to the first memory.

17. A network switch as recited in claim 7, wherein said at least one address pool

further comprises:

a cell free address pool connected to the first memory controller; and

a slot free address pool connected to the second memory controller.

18. A network switch as recited in claim 6, said network switch further comprising:

a cell free address pool unit in connection with the first memory controller;

a slot free address pool unit in connection with the second memory controller; and

a scheduler connected to the first memory controller and the second memory controller.

19. A network switch as recited in claim 18, wherein the cell free address pool unit further comprises a cell free address pool and a cell free address pool

controller connected to the cell free address pool.

20. A network switch as recited in claim 19, wherein the cell free address pool controller is configured to receive and release free addresses from the cell free address pool unit for use in storing cells in the first memory.

21. A network switch as recited in claim 18, wherein the scheduler transmits a token between at least two egress managers in accordance with a predetermined algorithm, thereby allowing the at least two egress managers to individually schedule an egress transmission of data when the token is present.

22. A network switch as recited in claim 18, wherein the slot free address pool unit

further comprises a slot free address pool and a slot free address pool controller connected to the slot free address pool.

23. A network switch as recited in claim 22, wherein the slot free address pool controller is configured to receive and release free slots from the slot free address pool for use in storing cells in the second memory.

24. A network switch as recited in claim 18, wherein the first memory controller receives and processes requests for storage of data in the first memory.

25. A network switch as recited in claim 18, wherein the second memory controller receives and processes requests for storage of data in the second memory.

26. A network switch as recited in claim 25, wherein the second memory controller receives requests from a slot assembly unit, the slot free address pool, a slot assembly unit, and a refresh requestor.

27. A method for storing data in a network switch, said method comprising the steps of:

receiving data to be transmitted to an egress at an input to a memory management unit;

formatting the data received as a linked list;

determining if the data is to be stored in a first memory or a second memory; and

storing the data in the first memory or the second memory based on the

determining step.

28. A method for storing data in a network switch as recited in claim 27, wherein the determining step further comprises the steps of:

determining if a cell count is less than a first predetermined threshold for the egress;

determining if a number of cells in the second memory is zero; and

determining if a number of cells in the first memory added to a number of cells remaining in an assembly is less than the first predetermined threshold.

29. A method for storing data in a network switch as recited in claim 27, wherein the step of storing data in the first memory further comprises the steps of:

initializing a cell count;

setting an in progress flag;

loading a first cell pointer into a memory controller;

incrementing the cell count;

storing a first cell in the local memory;.

30. A method for storing data in a network switch as recited in claim 29, further comprising the steps of

incrementing the cell count;

storing a next cell in the first memory;

determining if a last cell bit is set; and

loading a next cell pointer and continuing to store cells if the last cell bit is determined not to be set.

31. A method for storing data in a network switch as recited in claim 27, wherein the step of storing data in the second memory further comprises the steps of initializing global storage of data and continuing global storage of data until a last slot is stored.

32. A method for storing data in a network switch as recited in claim 31, wherein the step of initializing global storage further comprises the steps of:

initializing a global cell count and setting an in progress flag;

incrementing the global cell count;

writing a first cell to a cell accumulation buffer;

determining if a last cell bit is set; and

loading a next cell pointer if the last cell bit is not set.

33. A method for storing data in a network switch as recited in claim 32, wherein the step of continuing global storage further comprises the steps of:

incrementing the global cell count;

writing a next cell to the cell accumulation buffer;

determining if the last cell bit is set;

continuing global storage of cells if the last cell bit is not set; and

clearing the in progress flag if the last cell bit is set.